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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,375	10/03/2003	Kuei-Ann Wen	N0113/PP/HH	4031

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SUGHRUE MION, PLLC
401 Castro Street, Ste 220
Mountain View, CA 94041-2007

EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 06/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,375	WEN, KUEI-ANN	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/678,375 filed 10/03/2003 and amendment filed 04/05/2006.

2. Claims 1-20 remain pending in the Application.

3. Applicant's arguments have been fully considered and are persuasive. However, upon further consideration, a new ground(s) of rejection is made in view of Imai et al. (US Patent 6,026,228).

Drawings

4. The drawings are objected to because Figure 2 representing circuit design information generating tool demonstrates components/elements of the tool including relationships and exchanging a data between them in particular order. As noted in Applicant's remarks of the amendment, "Each line connecting two elements may be a one or two-way connection to enable information flow in either or both directions". Examiner requires showing it on the Figure 2. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be

necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 1-20 are objected to because of the following informalities:

- there is insufficient antecedent basis, such as preambles of claims 1 and 10 states "A **modularized** circuit design" and preambles of claims 2-9 and 11-20 being dependent from claims 1 and 10 state "The **modulated** circuit design information".

- claims 1 and 10 formulated unclear to what Applicant intent to mean in term of using a term "working integrated circuit" in third limitation (claim 1) and fourth limitation (claim 10). It's unclear if this "working integrated circuit" the same as "an integrated circuit" mentioned in the preambles of claims 1 and 10.

- claim 1 line 16 after "information" insert –of--

- claim 10 line 2 after "module" insert –s--

- claim 3 line 4 after "information file" insert –s--

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3-8, 10, 12-17, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Imai et al. (US Patent 6,026,228).

With respect to claim 1 Imai et al. teaches a modularized circuit design generating tool for designing an integrated circuit having a plurality of interconnected functional modules within a method and apparatus for integrated circuit design (col. 3, ll.11-16) including database apparatus using variety of modules as constituent elements (col. 5, ll.38-42), comprising a circuit module design database including circuit design an corresponding specification information of functional modules of at least two categories within database apparatus using **variety of modules** as constituent elements (col. 5, ll.38-42) as database system 10 as shown on the Fig. 3 (col. 7, ll.45-50) within database (FHM-DB) as shown on the Fig. 4, wherein various modules can be classified as shown in the Fig. 5, which is stored in the database 11 as information data describing each fictional module (specification) (col. 9, ll.13-16), wherein at least one category of the functional modules includes design information of circuit modules of at least two different specifications within various of modules along with the information data for each type of module having multiple classes (categories) (col. 9, ll.24-26); an element selection means allowing user to select suited circuit modules from the circuit module design database according to particular specifications of functional elements to be included into the integrated circuit to be designed within apparatus for integrated circuit design operated by a designer, wherein designer specifies constraints and generates

description data and instances of the object of design (modules) (col. 5, ll.44-47; ll.56-57) and to include circuit design and specification information corresponding to the selected circuit modules into circuit design information file of the circuit to be designed within description storage unit 18 shown on the Fig. 3 to store description data (specification information) of selected modules as constituent elements of the designed integrated circuit (col. 7, ll.51-53); a circuit module connection means to define connections between or among selected circuit modules according to features of each selected circuit module and thereby provides a circuit design of a working integrated circuit comprising the circuit modules within floorplanner 24 shown on the Fig. 3 (col. 7, l.54) for placing selected by the designer modules on the layout and connecting them to obtain design integrated circuit (col. 8, ll.28-31); a memory to store circuit design information of the working integrated circuit and of all selected circuit modules and information of connections between and/or among the selected circuit modules within output unit 56 as shown on the Fig. 4, wherein each selected by the designer module is registered along with the related to selected module information data (specification) for generated design integrated circuit (col. 10, ll.8-10; ll.31-33); and a file converting means to convert the circuit design information so obtained into an applicable format within synthesis unit 28 shown on the Fig. 3 to generate description data of the design integrated circuit in the format, wherein the design integrated circuit can be changed/corrected by designer or edition unit 16 shown on the Fig. 3 (col. 8, ll.51-61).

With respect to claim 10 Imai et al. teaches a method for designing an integrated circuit having a plurality of functional circuit modules by using modularized circuit

design information within a method and apparatus for integrated circuit design (col. 3, ll.11-16) including database apparatus using variety of modules as constituent elements (col. 5, ll.38-42), comprising: providing a circuit module design database including design information of functional circuit modules of at least two categories within database apparatus using **variety of modules** as constituent elements (col. 5, ll.38-42) as database system 10 as shown on the Fig. 3 (col. 7, ll.45-50) within database (FHM-DB) as shown on the Fig. 4, wherein various modules can be classified as shown in the Fig. 5, which is stored in the database 11 as information data describing each fictional module (specification) (col. 9, ll.13-16), wherein at least one category of the functional circuit modules includes design information of circuit modules of at least two different specification within various of modules along with the information data for each type of module having multiple classes (categories) (col. 9, ll.24-26); selecting from the design database suited functional circuit modules according to particular specifications of functional elements to be included into the integrated circuit to be designed within apparatus for integrated circuit design operated by a designer, wherein designer specifies constraints and generates description data and instances of the object of design (modules) (col. 5, ll.44-47; ll.56-57); including functional circuit design and specification information corresponding to the selected functional circuit modules into circuit design information file of the circuit to be designed within description storage unit 18 shown on the Fig. 3 to store description data (specification information) of selected modules as constituent elements of the designed integrated circuit (col. 7, ll.51-53); defining connections between or among selected circuit modules according to features

of each selected circuit module to thereby provide a circuit design of a working integrated circuit comprising the selected circuit modules interconnected by the connections within floorplanner 24 shown on the Fig. 3 (col. 7, l.54) for placing selected by the designer modules on the layout and connecting them to obtain design integrated circuit (col. 8, ll.28-31); and converting circuit design information so obtained into an applicable format within synthesis unit 28 shown on the Fig. 3 to generate description data of the design integrated circuit in the format, wherein the design integrated circuit can be changed/corrected by designer or edition unit 16 shown on the Fig. 3 (col. 8, ll.51-61).

With respect to claims 3-8, 12-17, 19 and 20 Imai et al. teaches:

Claims 3 and 12: wherein the circuit design information database comprises a group of circuit design information files for central processing unit, a group of circuit design information files for processing element, a group of design information files for memory circuit and a group of circuit design information file for interfacing circuit as shown on the Fig. 5, which is FHM database and stored in DB storage 11 shown on the Fig. 3 and includes data information of processor, a computational module, control module, a storage module, a communicational module etc. (col. 9, ll.38-41);

Claims 4 and 13: wherein the group of circuit design information files for central processing unit comprises core circuit design information for at least two central processing units different in operational speed, length in instruction or bus width with each other as shown on the Fig. 5, wherein data information of different classes of processors is stored each having different set of parameters as shown on the Fig. 6

(col.9;ll.42-44);

Claims 5 and 14: wherein the group of circuit design information files for processing circuit comprises circuit design information for at least two processing elements different in function as shown on the Fig. 5, wherein the data information of different computational modules (processing circuit) is stored, wherein different modules having different functions, such as ALU or multiplier, for example;

Claims 6 and 15: wherein the group of circuit design information files for processing circuit comprises circuit design information for at least one codec, at least one filter and at least one modulator as shown on the Figs. 5 and 6 demonstrating data information for multiple classes of modules stored in the database each having multiple set of parameters for each class of module (col. 9, ll.38-45);

Claims 7 and 16: wherein the group of circuit design information files for memory circuit comprises circuit design information for at least two types of memory different in memory space as shown on the Figs. 5 and 6 demonstrating data information for multiple classes of modules stored in the database each having multiple set of parameters for each class of module (col. 9, ll.38-45);

Claims 8 and 17: wherein the group of circuit design information for interfacing circuit comprises circuit design information for at least two interfacing circuits different in function as shown on the Figs. 5 and 6 demonstrating data information for multiple classes of modules stored in the database each having multiple set of parameters for each class of module including variety of interface modules (col. 9, ll.38-45);

Claim 19: a memory stored with circuit design information generated from the

method of any of claims 10-18 within output unit 56 as shown on the Fig. 4, wherein each selected by the designer module is registered along with the related to selected module information data (specification) for generated design integrated circuit (col. 10, ll.8-10; ll.31-33);

Claim 20: a circuit prepared with circuit design information generated from the method of any of claims 10-18 within output unit 56 as shown on the Fig. 4, wherein each selected by the designer module is registered along with the related to selected module information data (specification) for generated design integrated circuit (col. 10, ll.8-10; ll.31-33).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 9 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai et al. as applied to claims 1 and 10 above, and further in view of Hakewill et al. (US Patent Application Publication 20050149898).

With respect to claims 2, 9, 11 and 18 Imai et al. teaches the limitations from which the claims depend. However Imai et al. lacks specifics regarding location of residing the database, design information of the interfacing circuits and converters stored in the database. Hakewill et al. teaches:

Claims 2 and 11: wherein the circuit module design information database comprises a communications tool connectable to a remote database within typical implementation of the database by residing on the server site using network environment with a client/server arrangements and integrated circuit design apparatus (paragraph [0139];

Claims 9 and 18: wherein the group of circuit design information for interfacing circuit comprises circuit design information for at least one A/D converter, at least D/A converter, a USB interface circuit and a PCMCIA interface circuit within variety of types of the integrated circuit designs including different types of peripherals, such as A/D converters, D/A converters, interfaces, for example (paragraph [0142]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Hakewill et al. to teach the specifics subject matter Imai et al. does not teach, because an improved method an apparatus is managing the configuration, design parameters and functionality of an integrated circuit design in which the instruction set can be interactively varied by the user (paragraph [0011]).

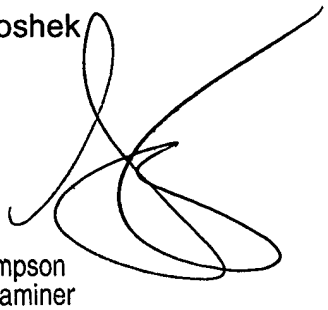
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Examiner
Helen Rossoshek
AU 2825



A. M. Thompson
Primary Examiner
Technology Center 2800